



Atty. Dkt. No. 039153-0256 (F0113)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Yu

Title: A PROCESS FOR
MANUFACTURING
TRANSISTORS HAVING
SILICON/GERMANIUM CHANNEL
REGIONS

Appl. No.: 09/599,141

Filing Date: 06/22/2000

Examiner: Roman, A.

Art Unit: 2812

CERTIFICATE OF MAILING I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, PO Box 1450, Alexandria, Virginia 22313-1450, on the date below. _____ (Printed Name) _____ (Signature) 9/21/03 _____ (Date of Deposit)

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT
UNDER 37 CFR §1.56

Commissioner for Patents
PO Box 1450
Alexandria, Virginia 22313-1450

Sir:

Submitted herewith on Form PTO-1449 is a listing of documents known to Applicant in order to comply with Applicant's duty of disclosure pursuant to 37 CFR §1.56. A copy of each listed document is being submitted to comply with the provisions of 37 CFR §1.97 and §1.98.

The submission of any document herewith, which is not a statutory bar, is not intended as an admission that such document constitutes prior art against the claims of the present application or that such document is considered material to patentability as defined in 37 CFR §1.56(b). Applicant does not waive any rights to take any action which would be appropriate to antedate or otherwise remove as a competent reference any document which is determined to be a *prima facie* art reference against the claims of the present application.

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TIMING OF THE DISCLOSURE

The listed documents are being submitted in compliance with 37 CFR §1.97(c), before the mailing date of either a final action under 37 CFR §1.113, a notice of allowance under 37 CFR §1.113, or an action that otherwise closes prosecution in the application.

RELEVANCE OF EACH DOCUMENT

All of the documents are in English.

Applicant respectfully requests that any listed document be considered by the Examiner and be made of record in the present application and that an initialed copy of Form PTO-1449 be returned in accordance with MPEP §609.

FEE

A fee in connection with submission of a supplemental information disclosure statement under 37 CFR §1.97(c) in the amount of \$180.00 in accordance with 37 CFR §1.17(p) is attached.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 CFR §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 06-1447. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 06-1447.

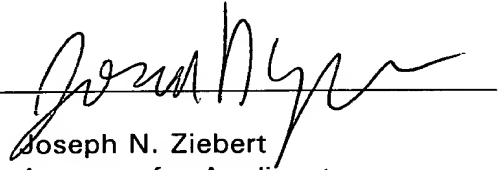
Respectfully submitted,

Date

8-29-03

FOLEY & LARDNER
777 East Wisconsin Avenue, Suite
3800
Milwaukee, Wisconsin 53202-5306
Telephone: (414) 297-5768
Facsimile: (414) 297-4900

By



Joseph N. Ziebert
Attorney for Applicant
Registration No. 35,421

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APPLICANT

Yu

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GROUP ART UNIT

2812

INFORMATION DISCLOSURE CITATION

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(Use several sheets if necessary)

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB- CLASS	FILING DATE IF APPROPRIATE
	A1	6,461,945	10/8/2002	Yu			
	A2	6,350,311	2/26/2002	Chin et al.			
	A3	6,319,799	11/20/2001	Ouyang et al.			
	A4	6,310,367	10/30/2001	Yagishita et al.			
	A5	6,268,640	7/31/2001	Park, et al.			
	A6	6,232,622	5/15/2001	Hamada			
	A7	6,190,975	2/20/2001	Kubo et al.			
	A8	6,172,381	1/9/2001	Gardner et al.			
	A9	6,133,082	10/17/2000	Masuoka			
	A10	6,130,144	10/10/2000	Verret			
	A11	6,031,269	2/29/2000	Liu			
	A12	6,022,785	2/8/2000	Yeh, et al.			
	A13	5,985,703	11/16/1999	Banerjee			
	A14	5,981,345	11/9/1999	Ryum, et al.			
	A15	5,936,280	8/10/1999	Liu			
	A16	5,910,015	6/8/1999	Sameshima, et al.			
	A17	5,856,225	01/5/1999	Lee et al.			
	A18	5,821,149	10/13/1998	Schuppen et al.			
	A19	5,766,989	6/16/1998	Maegawa et al.			
	A20	5,753,541	5/19/1998	Shimizu			
	A21	5,689,136	11/18/1997	Usami et al.			
	A22	5,683,934	11/4/1997	Candelaria			
	A23	5,675,185	10/7/1997	Chen et al.			
	A24	5,612,552	3/18/1997	Owens			
	A25	5,591,653	1/7/1997	Sameshima, et al.			
	A26	5,581,101	12/3/1996	Ning et al.			
	A27	5,554,870	9/10/1996	Fitch et al.			

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EXAMINER

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- * EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include any copy of this form with next communication to applicant.

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U.S. PATENT DOCUMENTS

A28	5,497,019	3/5/1996	Mayer et al.			
A29	5,482,877	1/9/1996	Rhee			
A30	5,461,250	10/24/1995	Burghartz et al.			
A31	5,451,798	9/19/1995	Tsuda et al.			
A32	5,420,048	5/30/1995	Kondo			
A33	5,414,288	5/9/1995	Fitch et al.			
A34	5,346,834	9/13/1994	Hisamoto et al.			
A35	5,321,286	6/14/1994	Koyama et al.			
A36	5,155,571	10/13/1992	Wang et al.			
A37	5,128,732	7/7/1992	Sugahara et al.			
A38	5,041,884	8/20/1991	Kumamoto et al.			
A39	5,036,374	7/30/1991	Shimbo			
A40	5,019,882	5/28/1991	Solomon et al.			
A41	5,008,211	5/16/1991	Yamazaki			
A42	4,996,574	2/26/1991	Shirasaki			
A43	4,994,866	2/19/1991	Awano			
A44	4,975,387	12/4/1990	Prokes et al.			
A45	4,849,033	7/18/1989	Vander Sande et al.			
A46	4,710,478	12/1/1987	Yoder et al.			
A47	4,697,333	10/6/1987	Nakahara			
A48	4,381,201	4/26/1983	Sakurai			
A49	4,272,880	6/16/1981	Pashley			
A50	4,174,521	11/13/1979	Neale			
A51	4,046,618	9/6/1977	Chaudhari et al.			


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FOREIGN PATENT DOCUMENTS

REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION	
						YES	NO
A52	JP-5-335482	12/1993	Japan				
A53	EP 0 334 682-A2	03/1989	European				
A54	3-288471	12/18/1991	Japan				
A55	61-180466	8/13/1986	Japan				

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

A56	"Smart-Cut: The Basic Fabrication Process for UNIBOND Soi Wafers" Herve, et al., March 3, 1997.
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				FILING DATE 06/22/2000		GROUP ART UNIT 2812	
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)							
	A56	"Sub-100nm Gate Length Metal Gate NMOS Transistors Fabricated by a Replacement Gate Process" By Chatterjee, December 7-10, 1997 IEEE.					
	A58	U.S. Patent Application Serial No. 09/599,270 entitled "A SOLID PHASE EPITAXY PROCESS FOR MANUFACTURING TRANSISTOR SHAVING SILICON/GERMANIUM CHANNEL REGIONS" " by Yu on 6/22/00. (Atty. Dkt. No. 39153-268)					
	A59	U.S. Patent Application Serial No. 09/817,580 entitled "METHOD OF LOCALLY FORMING A SILICON/GERMANIUM CHANNEL LAYER" by Yu on 03/26/2001. (Atty. Dkt. No. 39153-428)					
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